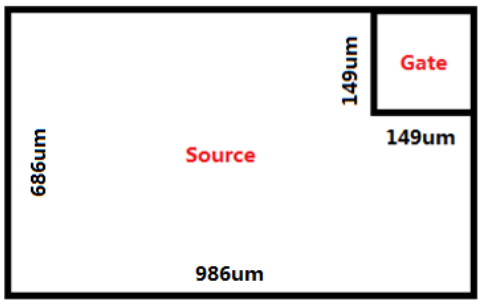
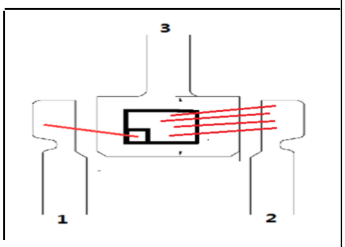


Die size：986μm x 686μm (including scribe line)
Gate：149μm x 149μm
Gross die / per 8” wafer =43500pcs

For SOT-23 package
Suggest Bonding wire：
Gate：1*42um Cu
Source：4*42um Cu



ii. Mechanical Data

Nominal Back Metal Composition, Thickness:	Ti- Ni - Ag, (1kA°-2kA°-10kA°)
Nominal Front Metal Composition, Thickness:	AlCU(0.004mm)
Wafer Diameter:	200mm, with 010 notch
Wafer Thickness:	175μm
Scribe line width	60μm
Passivation	SiON

iii. Wafer Key Electrical Characteristics （CP Test）

Parameter	Description	Min.	Typ.	Max.	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-12V	-18V		V_{GS} = 0V, I_D = -250μA
$ID_{(Device Ref.)}$	Continuous Drain Current			-5A	T_J = 25°C
$R_{DS(on)}$	Static Drain-to-Source On-Resistance		23 mΩ	32 mΩ	V_{GS} =-4.5V, I_D =-1A
			35 mΩ	50 mΩ	V_{GS} =-2.5V, I_D =-0.5A
$V_{GS(th)}$	Gate Threshold Voltage	-0.4V	-0.7V	-1 V	V_{DS} =V_{GS}, I_D = -250μA
I_{DSS}	Drain-to-Source Leakage Current			1μA	V_{DS} =-12V, V_{GS} = 0V, T_J = 25°C
I_{GSS}	Gate-to-Source Leakage Current			±100nA	V_{GS} = ±12V

iv. Rdson after SOT-23 package

$R_{DS(on)}$	Static Drain-to-Source On-Resistance		29 mΩ	40 mΩ	V_{GS} =-4.5V, I_D =-5A
			40 mΩ	60 mΩ	V_{GS} =-2.5V, I_D =-4A